13 - MOSFETs Advanced Name:_____

In-Class Problems

(1) Lets calculate threshold voltage for a real MOSFET.

The gate electrode 'metal' is n+ poly Silicon.

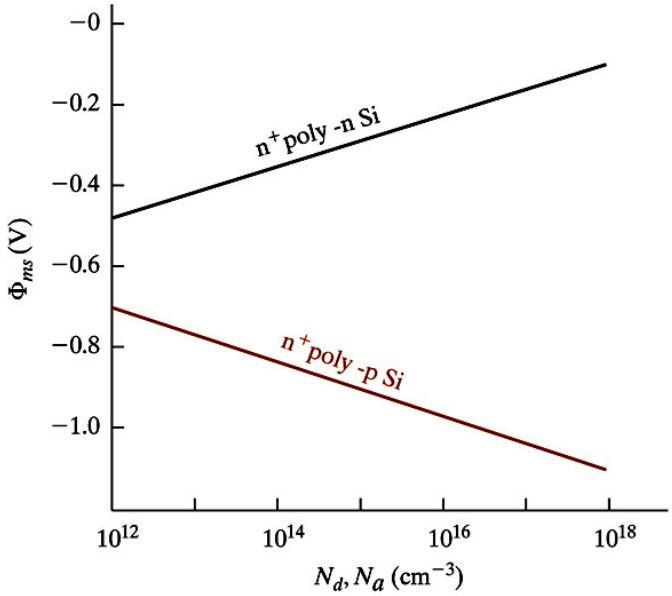
The substrate is p Si with Na=10^{16}/cm^3, and the Fermi level for the p Si is 0.35 eV below the intrinsic (undoped) Fermi level.

Under the gate oxide, the maximum achievable depletion width into the p Si is 300 nm.

The gate oxide has a capacitance of 200 nF/cm^2.

There is no interface charge (Qi).

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$



Calculate the threshold voltage for this n-MOSFET device.
Remember, some MOSFETs can be close to 'on' or normally 'on' at Vg=0 because of the difference between the metal and semiconductor work functions.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

N_d, N_a (cm^{-3})

(a) [15 pts] Calculate the threshold voltage for this n-MOSFET device.

* added

Remember, some MOSFETS can be normally 'on' at $V_g = 0$ because of the effect of ϕ_{ms}.

$$V_T = -0.9\,V - 0 + \frac{4.8\times10^{-8}}{2\times10^{-7}} + 2\cdot0.35 = 0.04\,V$$

$$Q_d = -qN_aW_m = -1.6\times10^{-19}\cdot10^{16}\cdot300\times10^{-7}$$
$$= -4.8\times10^{-8}\ C/cm^2$$

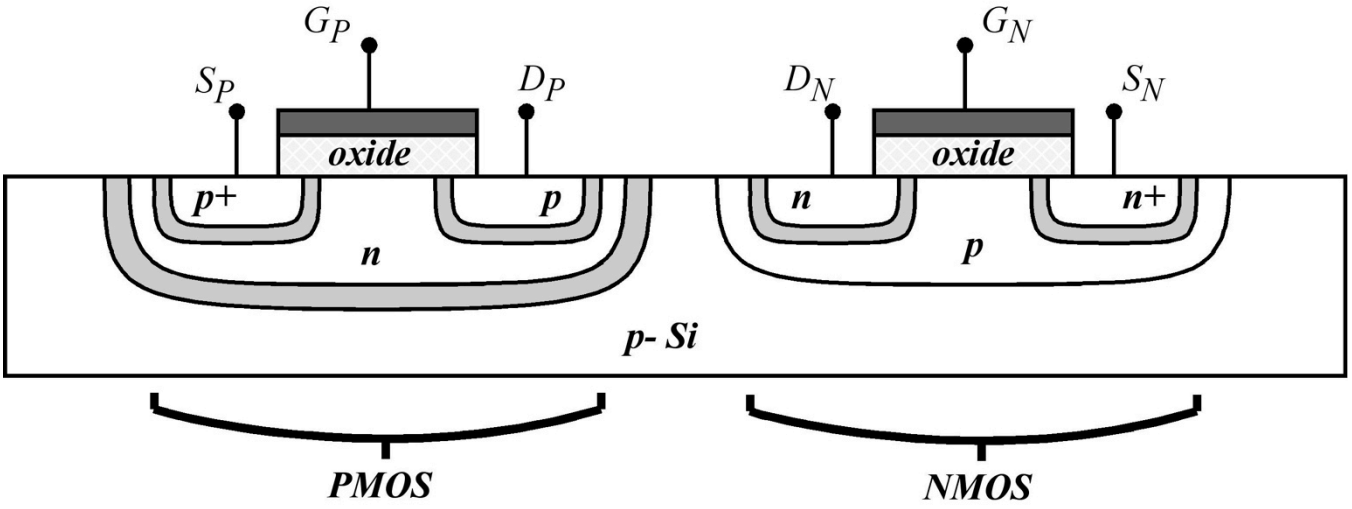
Note – this should be 0.95 to 1.0 for Phi(ms). Above has 0.9 which is a bit off (depends on accuracy of tracing values off of the graph).

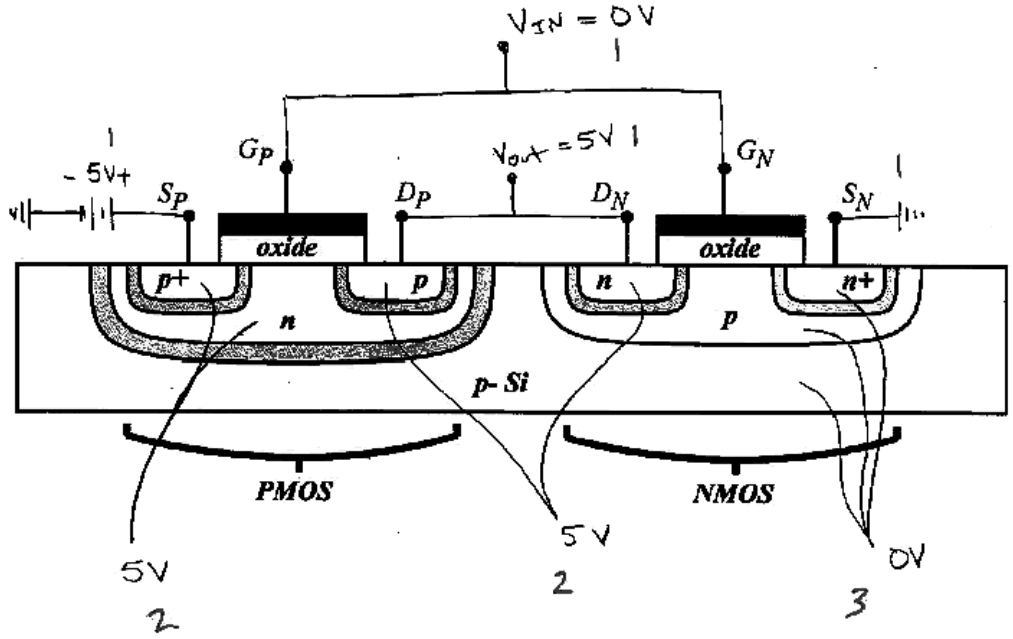
(2) The following is for an ideal pair of NMOS and PMOS devices that form the basis for a logic inverter. Perform the following. QUALITATIVE ANSWERS / NO EQUATIONS CALCULATIONS ARE NEEDED.

(a) Lets do this problem like we did in lecture first…

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw a ground on the NMOS source and +5V on the PMOS source.

SECOND: using lines with arrows, or directly on the diagram, label as many voltages as possible on each <u>semiconductor region (there are 7 different regions below)</u> for the case of 0V applied to V_{IN}, and also label the voltage at V_{OUT} (just label the voltages at 0V, or 5V, and don't worry about labeling the voltages close to the gate oxide).





(b) Now, lets mix it up a bit…

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw -10 V on the NMOS source and -5V on the PMOS source.

SECOND: label the diagram similar to how you did for part (a), but do it for the case where the output voltage is -5 V. Note, now you have to label the input voltage too! You may only label it with voltages such as -15V, -10V, -5 V, 0V, 5V, 10V, 15V. Do not use any more voltage than is needed to exceed Vth.

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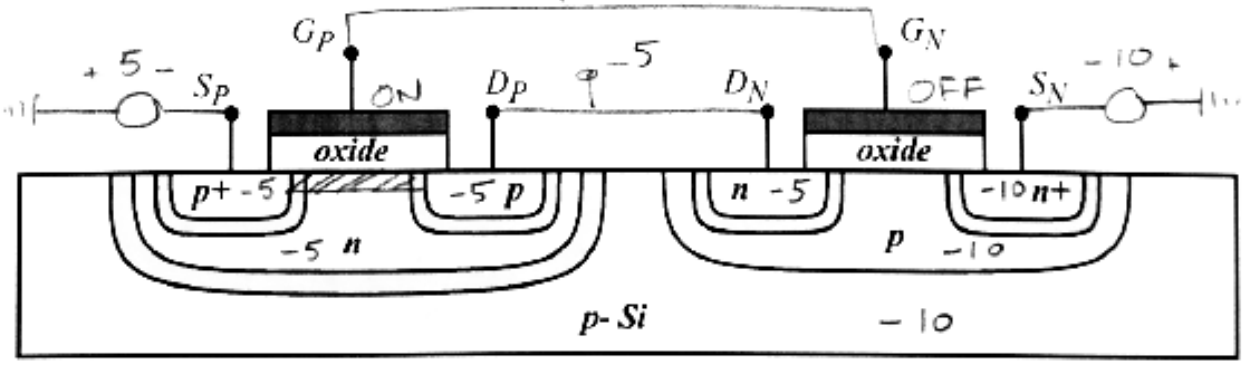


2 points each

same as (a) just subtract -10V from everything!

(3) Let's play SHIFT or FLIP! Which of the terms in the equation have no change, SHIFT in magnitude, or which FLIP in polarity when we switch between NMOS and PMOS (make sure you understand WHY).

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

shifts flip +/- for PMOS

(4) Something students make mistakes on all the time… For only the ideal terms in the threshold equation (shown below), students get confused often on the +/- signs. Here is how to sanity check your work…

Let's say we have a PMOS device, which means NEGATIVE gate voltage to create POSITIVE charge on the other side of the MOS capacitor. If the terms below are ALWAYS 'the price you have to pay' to turn a MOSFET on (increase your threshold voltage), then both parts of the equation must be what sign (+ or -)?

$$V_T = -\frac{Q_{d,\max}}{C_i} + 2\phi_f$$

Answer – the both MOST be negative. If it were NMOS, they would both have to be positive! They don't help you lower threshold voltage, they ALWAYS must increase it!

(5) A bit more review….

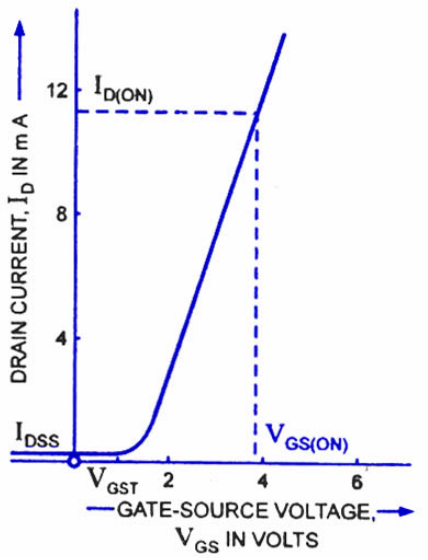
(a) for the 'transfer' curve on the left (Id vs. Vgs is always called a 'transfer' curve), why above threshold is I_D linear with increasing Vgs? *Remember, creation of inversion charge with changing surface potential is exponential (a Fermi distribution type function), but there is a simpler reason why change in the actual drain current is linear with external applied voltage. Think of a basic law that governs capacitors…*

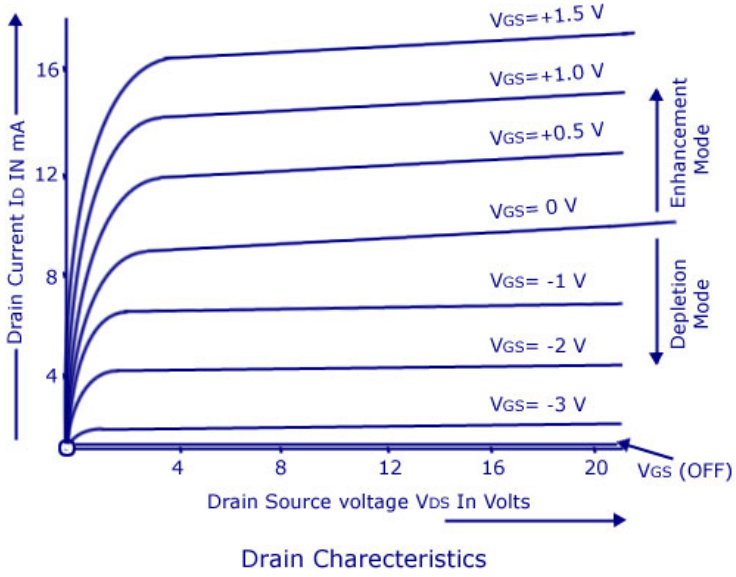
Answer – Is because of the law of Q=CV!!

(b) see the curve on the right…. After the lecture for today, we now know that with all the real threshold voltage terms for a MOSFET it can actually be ON even with 0V applied to the gate. For the curve at right, is this NMOS or PMOS? And where it says V_{GS} (OFF) on the curve, in what state is the MOSFET (draw a simple diagram to explain).

Answer – NMOS

Answer - It is in depletion (right before inversion starts).





(6) For an ideal PMOS device (formed on n-type Si) with a 10 nm gate oxide, W_m=300 nm, and area of gate = 100x100 nm^2, provide the following:

(a) the maximum capacitance seen by the gate electrode occurs for (check all that apply)
_X_ enough positive voltage for accululation, applied to the gate.
___ any amount of negative voltage, applied to the gate.
_X_ voltage greater than the threshold voltage, applied to the gate.
___ 0 V up to the threshold voltage, applied to the gate.

(b) now calculate the maximum capacitance <u>per unit area</u> seen by the gate electrode (remember, gate oxide is SiO2, which has relative dielectric constant (permittifity) of 3.9):

Ci = *insulator* capacitance (i.e. the insulator material, which is the silicon dioxide or SiO2)

Ci = $e_{SiO2}e_0/t$ = 3.9 * 8.854E-14 F/cm / 10 E-7 cm = 3.45E-7 F/cm2

(If you calculated the actual capacitance, and included area, this would be the answer 3.45E-7 F/cm^2 x (100E-7 cm)^2 = 3.45E-17 F)

(c) now calculate the minimum capacitance seen by the gate electrode (the actual capacitance, not the capacitance per unit area):

Cd = *the depletion* capacitance (i.e. the capacitance of the depleted semiconductor layer under the channel right before inversion, which is also when the depletion width W is maximized)

Cd = $e_{Si}e_0/W$ = 11.8 * 8.854E-14 F/cm / 300 E-7 cm = 3.48E-8 F/cm2

Now, at minimum capacitance C_{min}, both of these capacitances are placed in series (oxide and depletion sandwiched together in series). So we can use simple series capacitance calculation:

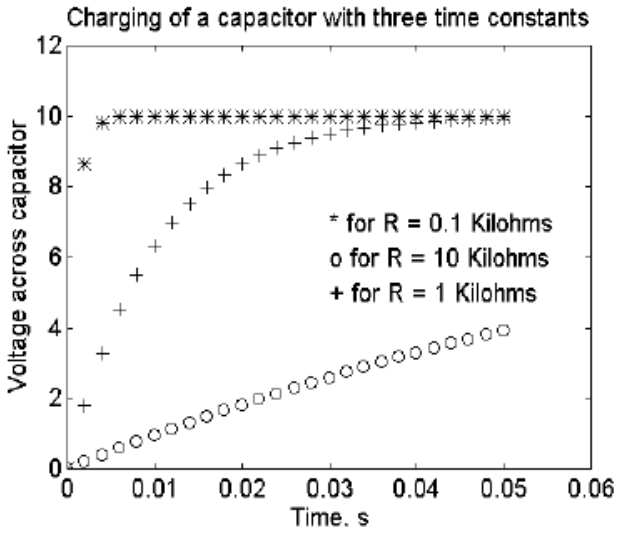
C_{min}= Cd Ci / (Cd + Ci) = 3.16 E-8 F/cm2 (makes sense, the smaller capacitor dominates the series capacitance)

Lastly multiply F/cm2 by gate area (cm2) to get just F : 3.16E-8 F/cm^2 x (100E-7 cm)^2 = 3.16E-18 F.

(7) Assume you make 3 batches of MOSFETs that when turned fully on they have a source-to-drain channel resistance of 1,10, or 100 MΩ.

(a) Revise the MATLAB code below to plot the voltage vs. time for these transistors as they charge up the next transistor which has a maximum gate capacitance of $3x10^{-17}$ F.

```
% Code for charging of an RC circuit
% From Attia – Elect. & Circ. Anal. Using MATLAB
c = 10e-6;
r1 = 1e3;
tau1 = c*r1;
t = 0:0.002:0.05;
v1 = 10*(1-exp(-t/tau1));
r2 = 10e3;
tau2 = c*r2;
v2 = 10*(1-exp(-t/tau2));
r3 = .1e3;
tau3 = c*r3;
v3 = 10*(1-exp(-t/tau3));
plot(t,v1,'+',t,v2,'o', t,v3,'*')
axis([0 0.06 0 12])
title('Charging of a capacitor with three time constants')
xlabel('Time, s')
ylabel('Voltage across capacitor')
text(0.03, 5.0, '+ for R = 1 Kilohms')
text(0.03, 6.0, 'o for R = 10 Kilohms')
text(0.03, 7.0, '* for R = 0.1 Kilohms')
```



(b) could you use your MOSTFETs to make a GHz computer chip?

___ yes, it looks like from my plot that charging time is on the order of ns, inverse of ns (time) is GHz (freq.)

___ no, it looks like from my plot that charging time is on the order of μs, inverse of μs (time) is MHz (freq.)

_X_ not even close, in a chip there are way too many transistors in series for a single logic operation, so have to be way faster than GHz for each individual transistor!